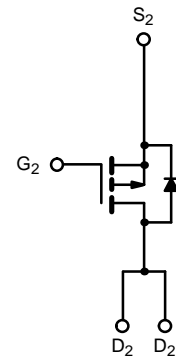
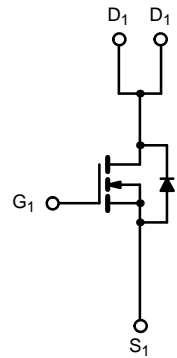
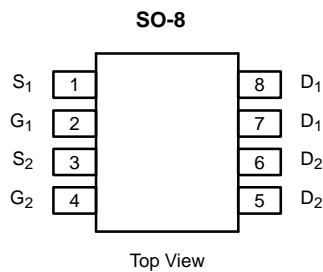




Complimentary 20-V (D-S) MOSFET

PRODUCT SUMMARY			
	V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
N-Channel	20	0.125 @ $V_{GS} = 10$ V	± 3.0
		0.250 @ $V_{GS} = 4.5$ V	± 2.0
P-Channel	-20	0.200 @ $V_{GS} = -10$ V	± 2.5
		0.350 @ $V_{GS} = -4.5$ V	± 2.0



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	V_{DS}	20	-20	V
Gate-Source Voltage	V_{GS}	± 20	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	± 3.0	A
		$T_A = 70^\circ\text{C}$	± 2.5	
Pulsed Drain Current	I_{DM}	± 10	± 10	
Continuous Source Current (Diode Conduction) ^a	I_S	1.6	-1.6	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.0	W
		$T_A = 70^\circ\text{C}$	1.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C}/\text{W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>



SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	1.0			V
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	-1.0			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 16 V, V _{GS} = 0 V	N-Ch			2	μA
		V _{DS} = -16 V, V _{GS} = 0 V	P-Ch			-2	
		V _{DS} = 16 V, V _{GS} = 0 V, T _J = 55 °C	N-Ch			25	
		V _{DS} = -16 V, V _{GS} = 0 V, T _J = 55 °C	P-Ch			-25	
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	N-Ch	10			A
		V _{DS} ≤ -5 V, V _{GS} = -10 V	P-Ch	-10			
		V _{DS} ≥ 5 V, V _{GS} = 4.5 V	N-Ch	2			
		V _{DS} ≤ -5 V, V _{GS} = -4.5 V	P-Ch	-2			
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 10 V, I _D = 1.0 A	N-Ch		0.07	0.125	Ω
		V _{GS} = -10 V, I _D = 1.0 A	P-Ch		0.12	0.200	
		V _{GS} = 4.5 V, I _D = 0.5 A	N-Ch		0.105	0.250	
		V _{GS} = -4.5 V, I _D = 0.5 A	P-Ch		0.22	0.350	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 3.0 A	N-Ch		4.8		S
		V _{DS} = -15 V, I _D = -3.0 A	P-Ch		3.0		
Diode Forward Voltage ^b	V _{SD}	I _S = 1.25 A, V _{GS} = 0 V	N-Ch		0.75	1.2	V
		I _S = -1.25 A, V _{GS} = 0 V	P-Ch		-0.8	-1.2	
Dynamic^a							
Total Gate Charge	Q _g	N-Channel V _{DS} = 10 V, V _{GS} = 10 V, I _D = 2.3 A P-Channel V _{DS} = -10 V, V _{GS} = -10 V, I _D = -2.3 A	N-Ch		7	25	nC
Gate-Source Charge	Q _{gs}		N-Ch		0.75		
Gate-Drain Charge	Q _{gd}		P-Ch		1.3		
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 20 V, R _L = 20 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _G = 6 Ω P-Channel V _{DD} = -20 V, R _L = 20 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _G = 6 Ω	N-Ch		6	15	ns
Rise Time	t _r		P-Ch		10	40	
			N-Ch		10	20	
Turn-Off Delay Time	t _{d(off)}		P-Ch		12	40	
			N-Ch		17	50	
Fall Time	t _f		P-Ch		20	90	
			N-Ch		10	50	
Source-Drain Reverse Recovery Time	t _{rr}		P-Ch		10	50	
		N-Ch		45	100		
					70	100	

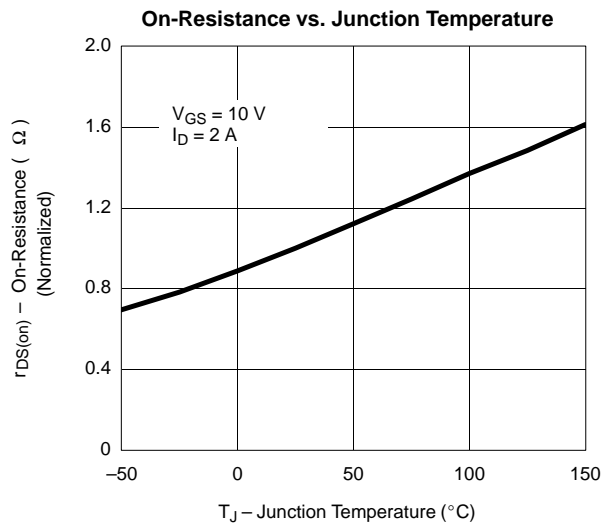
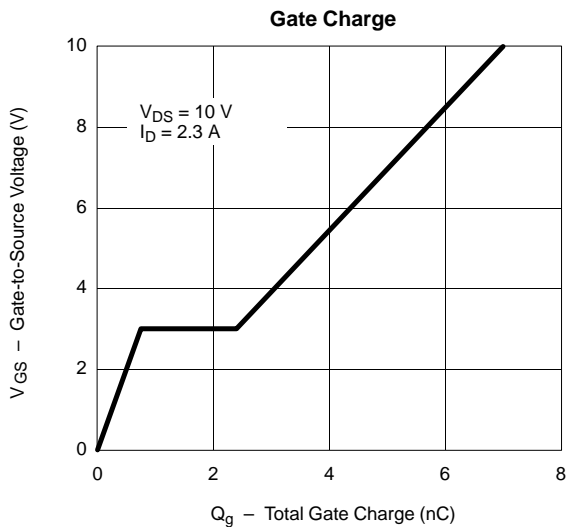
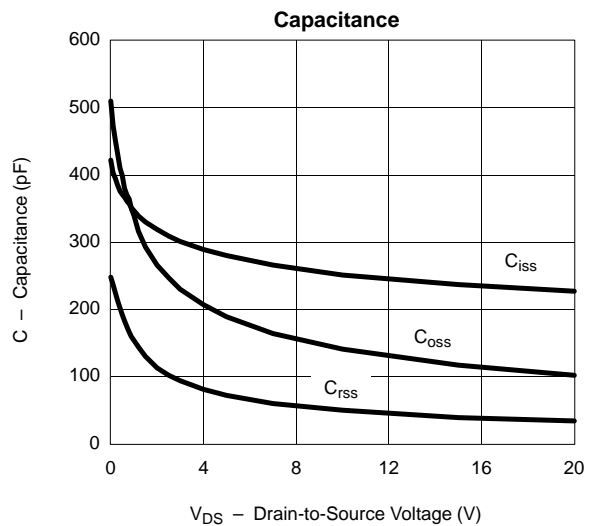
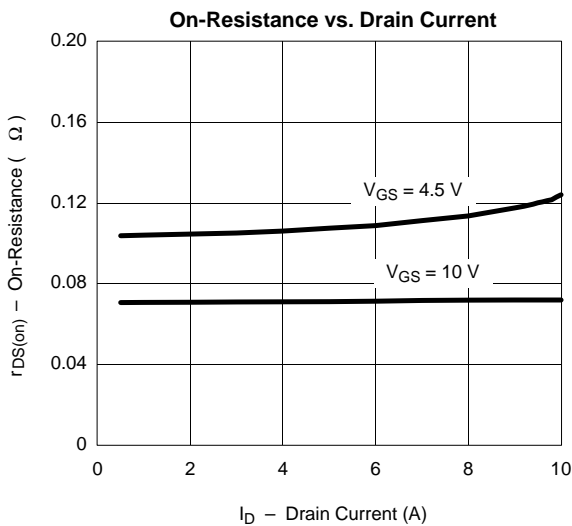
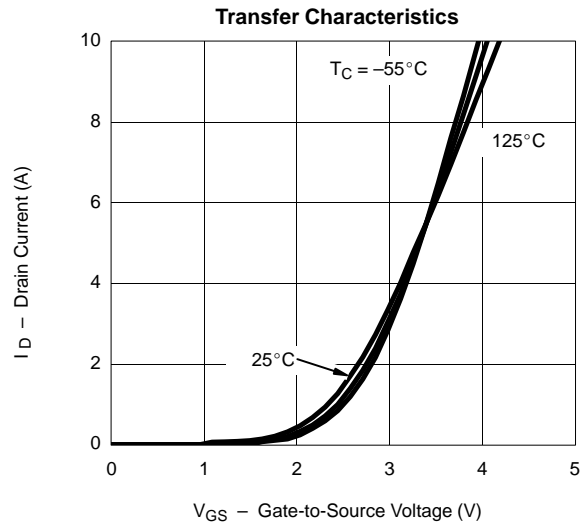
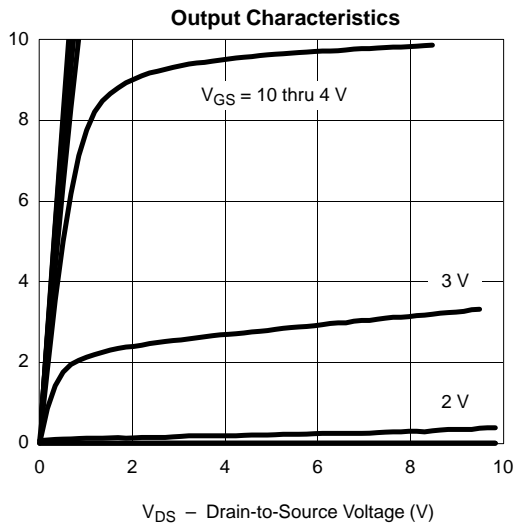
Notes

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

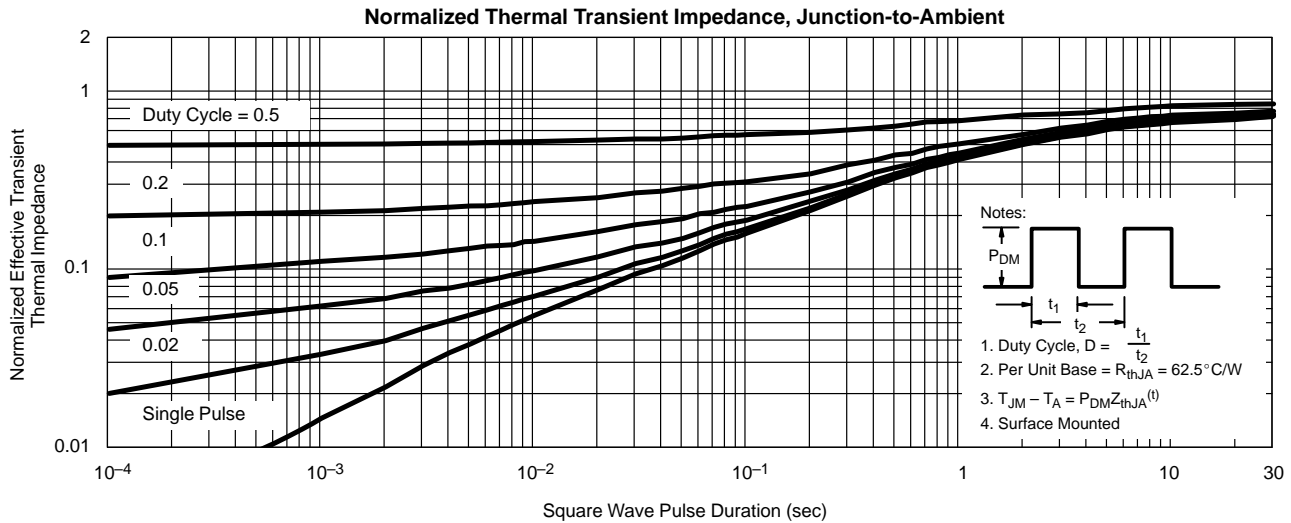
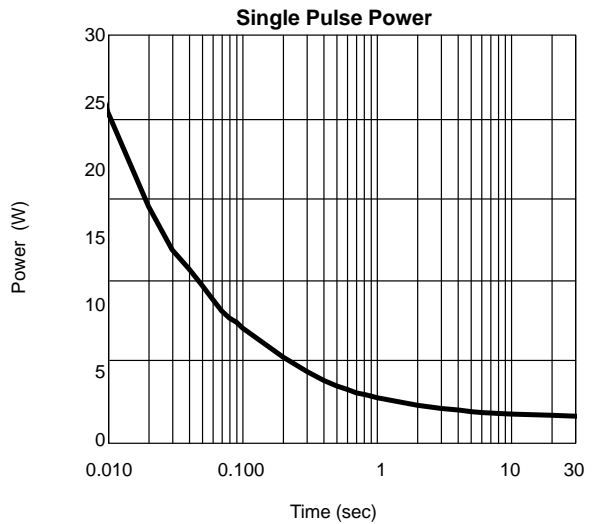
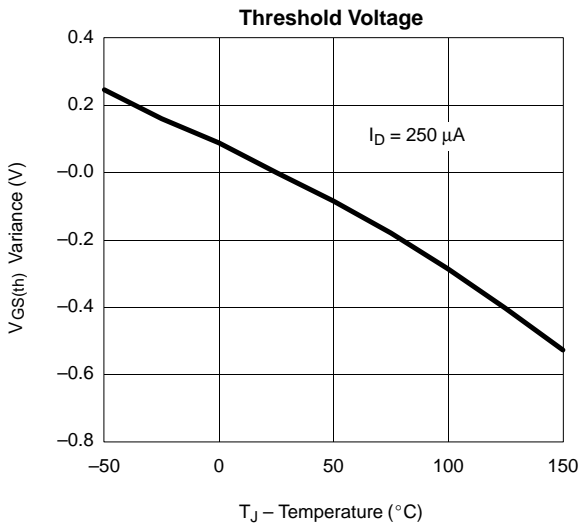
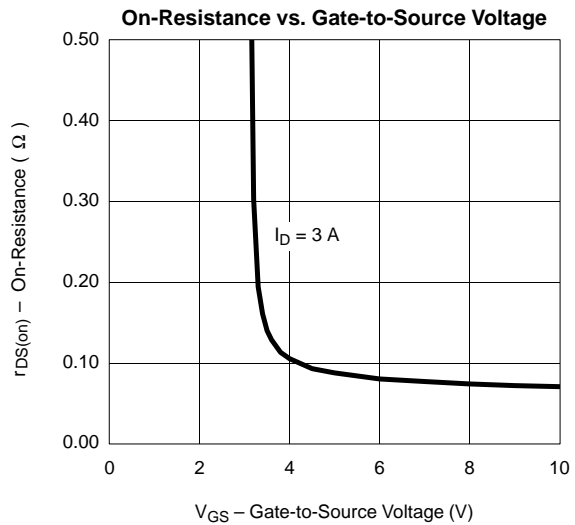
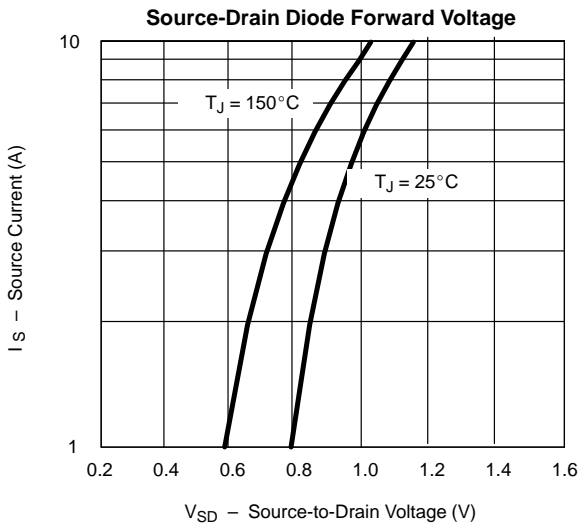


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

N-CHANNEL

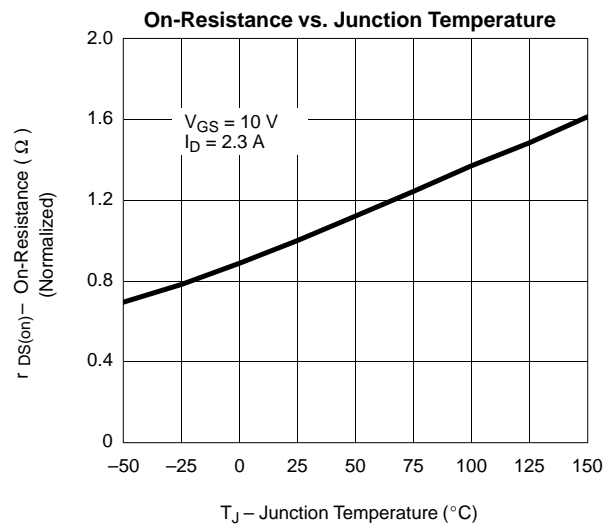
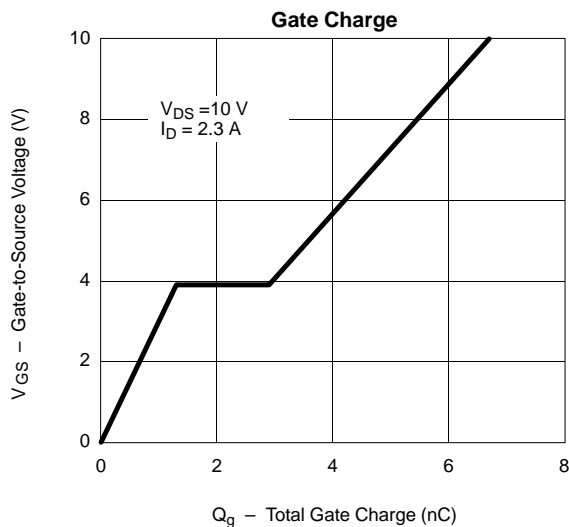
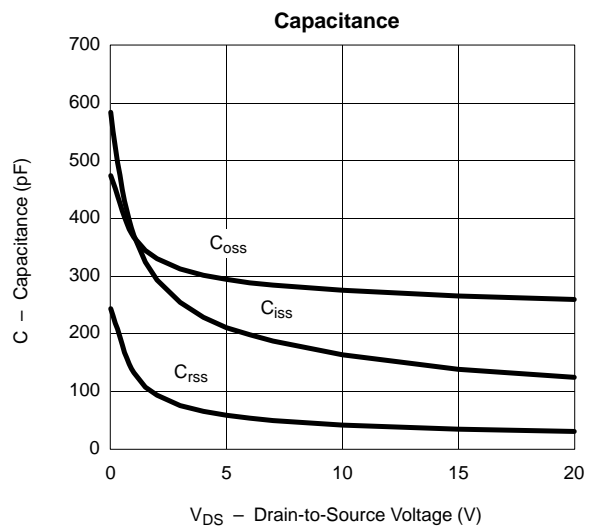
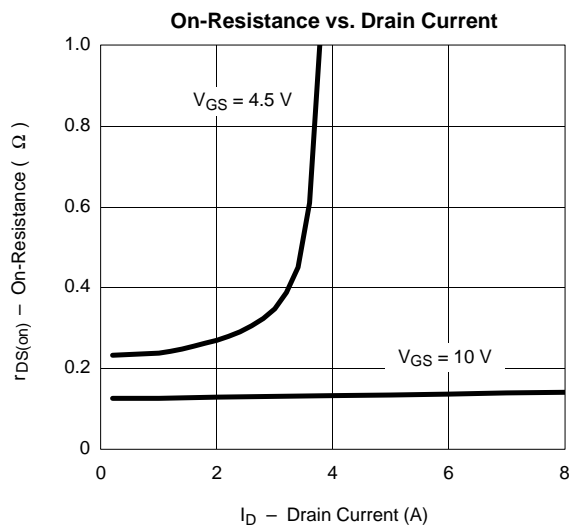
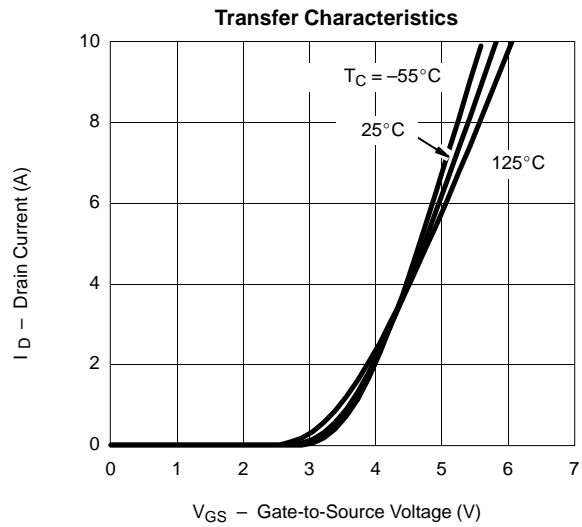
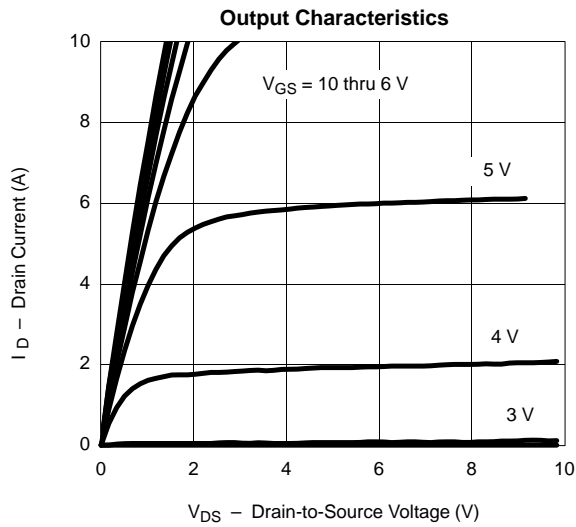


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL

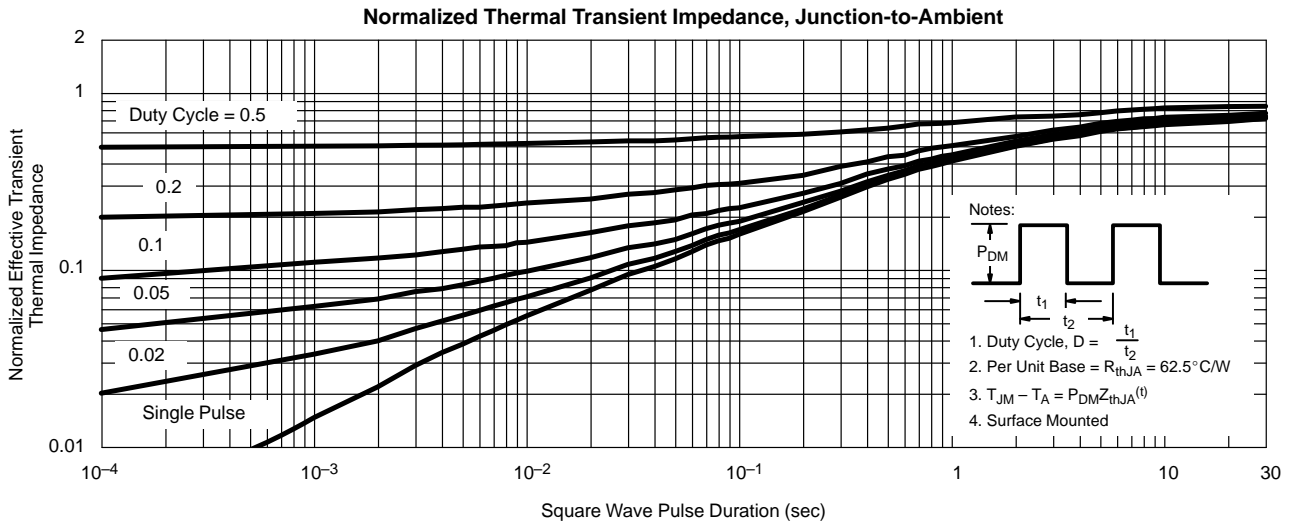
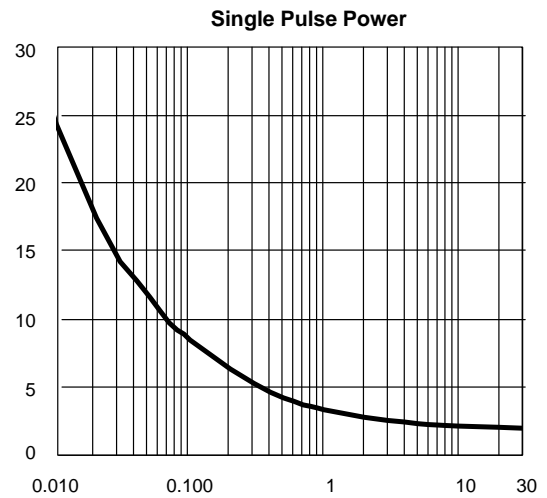
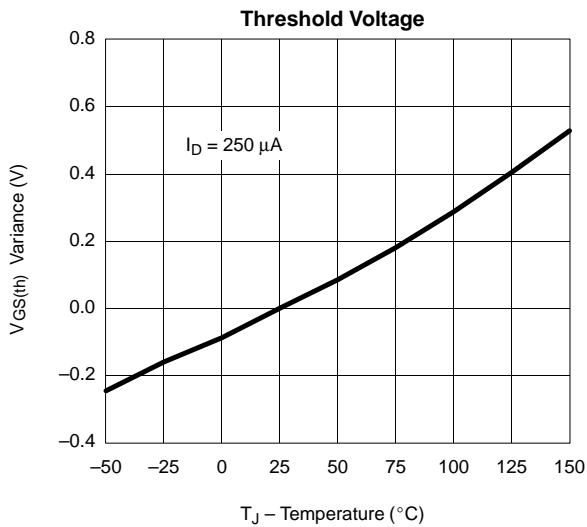
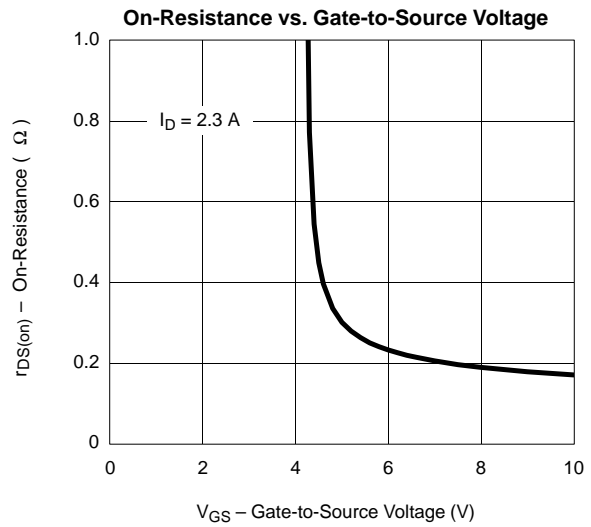
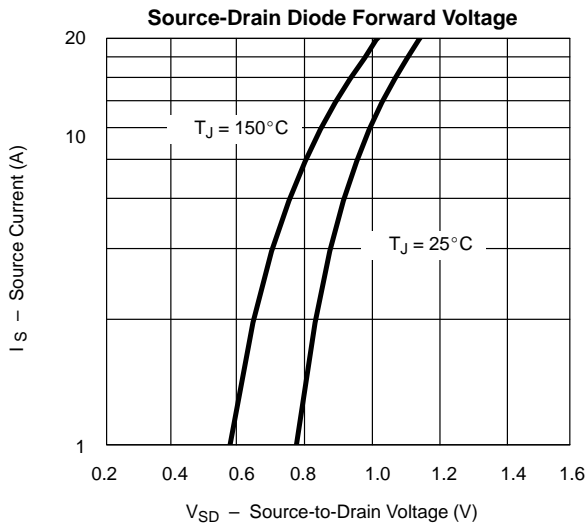




TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) P-CHANNEL





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